

REMARKS

In the foregoing amendments, applicant's specification was amended to correct a typographical error, as requested in the outstanding Office Action. In addition, Claims 1-5 were amended, and Claims 6-9 were added to the application. Attached hereto is a marked-up version of the changes made to specification and Claims 1-5 by the current amendment. The attached pages are captioned **"VERSION WITH MARKINGS TO SHOW CHANGES MADE."** Claims 1-9 are in the application for consideration by the Examiner.

The Official Action set forth an objection of the drawings, because they do not include the following reference signs mentioned in the description:

1. Page 22, line 10 of the specification refers to a surface roughness "R" which is not represented in the figures.
2. Page 32, lines 19 and 20 of the specification referred to an interval "X" and a maximum length "Y" which are not shown in the figures.

In addition, the Official Action stated that Figures 6 and 7 should be designated by legends such as -- Prior Art -- because both figures are disclosed in Japanese 11156563 as Figs. 1 and 2.

Together with this Response, applicant is filing a Request for Approval of Drawing Changes where Figs. 6 and 7 are designated as -- Prior Art --. In addition, it is proposed that Figs. 6 and 7 be amended to show the interval X" and the maximum length "Y," as marked in red thereon and as discussed in

the Office Action. It is respectfully requested that the Examiner approve the attached Request for Approval of Drawing Changes.

While the Official Action stated that the drawings should show the surface roughness "R," applicant respectfully requests that the Examiner reconsider and withdraw this requirement. Typically, the surface roughness "R" is not shown in the drawings of the type in question, because it is difficult to do so in a meaningful manner. The surface roughness "R" is a parameter used to express the roughness of a surface, which is calculated by the formula shown on page 15, line 16. Typically, the surface roughness "R" is less than several μm , while the wafer can have a width of about 600 μm . Thus, it would be very difficult to show the surface roughness "R" in any meaningful manner in the drawings, because it is so small relative to the wafer. Thus, it is believed that any showing of the surface roughness "R" in the drawings would be misleading to one of ordinary skill in the art. For such reasons, applicant respectfully requests that the Examiner reconsider and withdraw the requirement of showing the surface roughness "R" in the drawings.

In paragraphs 5 and 6 of the Official Action, Claims 1-5 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Specifically, the Official Action stated that the phrase "very small" is a relative term that does not describe the scope of the claim. In the foregoing amendments, the phrase "very small" was removed from applicant's claims. Applicant respectfully submits that the claims, as amended, particularly point out and distinctly

claim the subject matter regarded as the invention within the meaning of 35 USC 112, second paragraph. Therefore, applicant respectfully requests that the Examiner reconsider and withdraw this rejection.

The Official Action set forth a rejection of Claim 1 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,418,467 of Iwai. The Official Action stated that Figure 7 of Iwai discloses a semiconductor wafer with very small dot marks (111b) on an inner wall face of a notch, indicated by the Official Action to be the place of 111b. The Official Action further argued that the production of the dot marks by a laser beam having a diameter of 1 to 13 μm is a product by process phrase and therefore the method of making the dot marks is not considered in the patentability of the product, the dot marks.

The Official Action also set forth a rejection of Claim 1 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,277,658B1 of Jeng *et al.* (Jeng). Figure 4B of Jeng was cited in the Official Action as teaching a semiconductor wafer with very small dot marks (22) on an inner wall face of a notch (18) formed on an outer peripheral face thereof. The Official Action stated that the method of making the dot marks does not affect patentability of the dot mark, as above.

The Official Action set forth a further rejection of Claim 1 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,268,641B1 of Yano *et al.* (Yano). Yano was cited in the Official Action as teaching a semiconductor wafer with a notch on an outer peripheral face. The Official Action

acknowledged that Yano does not teach very small dot marks on an inner wall face of a notch, but argued that it would have been obvious to have moved the marks on a side surface portion into the notch. The Official Action also stated that the method of making the dot marks does not affect patentability of the dot mark, as above.

The Official Action set forth a rejection of Claims 2-5 under 35 U.S.C. 103(a) as being unpatentable over Yano in view of U.S. Patent No. 6,004,405 of Oishi *et al.* (Oishi). The Official Action argued that it would have been obvious to have used the chamfered edge as taught by Oishi with the semiconductor of Yano to have obtained the invention as a whole. The Official Action noted the marks placed on the chamfered edge of Oishi are 10-500 μm in length (col. 2, lines 1-6).

Applicant respectfully submits that the teachings of Iwai, Jeng, Yano and/or Oishi either taken alone or in combination do not contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103.

The prior art rejections set forth in the Official Action rely upon two issues, a very expansive interpretation of the phrase “very small” and an argument that the use of a laser beam having a diameter of 1 to 13 μm does not affect the patentability of the dot marks themselves. Since none of the marks proposed by the prior art are remotely close in size to the sizes of the present

claims, applicant respectfully submits that none of these teachings can contemplate or suggest the presently claimed invention.

For example, the specification of Iwai speaks not to making very small dot marks, but purposely proposes making the alignment marks as large as possible. In other words, the teachings of Iwai are discussing an alignment mark, which needs a certain area and which is quite different from the presently claimed dot mark having a maximum length of 1 to 13 μm . See, for example, Col. 5, lines 33-39, of Iwai, which discloses alignment marks of about 100-200 μm in size. For these reasons, applicant respectfully submits that the teachings of Iwai are not pertinent to the presently claimed invention.

While the Official Action indicated otherwise, it is respectfully noted that the item 18 in Fig. 2 of Jeng is not a notch. Item 18 in Jeng is a portion of ring 16 contacting the wafer 20. An alignment notch 24 and monitor marks 22 are shown in Fig. 2 of Jeng. The monitor marks of Jeng are very large and of sufficient size to accommodate several monitor squares, each of which is 0.536 millimeters. Therefore, these monitor marks are not relevant to the presently claimed invention. While the teachings of Jeng propose a mark on the surface of the wafer, these teachings are silent with respect to marks on an inner surface of the wafer, as required in the present claims. Therefore, applicant respectfully submits that the teachings of Jeng cannot contemplate or suggest the presently claimed invention.

The teachings of Yano propose an indicator 16 on a declined portion 14 of a wafer. However, Yano teaches at column 8, lines 26-36, that it is preferable to mark an indicator 16 other than a notch. Thus, the presently claimed invention, which is directed to marking an indicator on an inner wall of a notch, is opposite to the disclosure or teachings of Yano. Therefore, applicant respectfully submits that such teachings cannot contemplate or suggest the presently claimed invention. For such reasons, applicant respectfully submits that the teachings of Yano cannot provide any motivation for moving any marks, as proposed therein, to the arrangement as set forth in the present claims.

The teachings of Oishi do not cure or rectify the deficiencies in the teachings of Yano. The teachings of Oishi propose a wafer without a notch. In particular, the teachings of Oishi propose at column 1, lines 26-23, that having a notch is not preferable. Thus, the teachings of Oishi teach away from the presently claimed invention and cannot be combined with the teachings of Yano, so as to arrive at the presently claimed invention. In particular, neither the teachings of Oishi nor Yano provide any motivation or suggestion to one of ordinary skill in the art for the present claimed invention. In fact, the presently claimed invention is directed to resolving the disadvantages of the inventions proposed by Oishi and Yano.

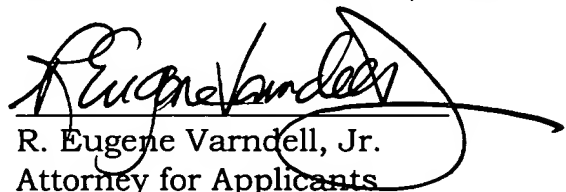
For the foregoing reasons, applicant respectfully submits that none of the teachings of Iwai, Jeng, Yano and Oishi, either taken alone or in combination,

contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103. Therefore, applicant respectfully requests that the Examiner reconsider and withdraw all the prior art rejections in the outstanding Office Action.

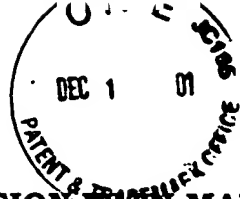
In view of the foregoing amendments and remarks, favorable consideration and allowance of Claims 1-9 are respectfully requested. While it is believed that all the claims in this application are in condition for allowance, should the Examiner have any comments or questions, it is respectfully requested that the undersigned be telephoned at the below listed number to resolve any outstanding issues.

In the event that this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge the fee therefor, as well as any deficiency in the payment of the required fee(s) or credit any overpayment, to our Deposit Account No. 22-0256.

Respectfully submitted,
VARNDELL & VARNDELL, PLLC


R. Eugene Varndell, Jr.
Attorney for Applicants
Registration No. 29,728

Atty. Case No. VX992060
106-A South Columbus St.
Alexandria, VA 22314
(703) 683-9730
V:\VDOCS\W_DOCS\DEC01\P052-2060 RS.DOC



VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 23, line 15, has been amended as follows:

-- A plane shape of the notch 1 is as shown by Fig. 2. In plane view, a longest dimension from a side face of the wafer W to a bottom portion of the notch 1 falls in a range of 1 to 1.25 mm, the bottom portion defines a circular arc face, a radius of curvature thereof is determined to be equal to or larger than 0.9 mm and an angle of an opening extended linearly from the bottom portion and opened at the side face of the wafer is 90 degree. Further, also an end edge of the opening is chamfered by [R] 0.9 mm and accordingly, a linear portion except the circular arc face portion of the bottom portion of the notch 1 becomes 0.669 mm at maximum. --

IN THE CLAIMS:

-- 1. (Amended) A semiconductor wafer with [very small] a dot [marks] mark having a maximum length of 1 to 13 μ m on an inner wall face of a notch formed on an outer peripheral face thereof [, wherein the dot marks are formed by irradiating a laser beam having a diameter of 1 to 13 μ m]. --

-- 2. (Amended) The semiconductor wafer according to Claim 1, wherein upper and lower edge line portions of the inner wall face of the notch are

respectively chamfered to thereby constitute upper and lower inclined faces and the dot [marks are] mark is formed on the inclined faces. --

-- 3. (Amended) The semiconductor wafer according to Claim 2, wherein an angle of an inclination of [the] at least one inclined face relative to the surface of the semiconductor wafer is equal to or smaller than 30 [degree] degrees. --

-- 4. (Amended) The semiconductor wafer according to Claim 2, wherein a surface roughness of [the] at least one inclined face is equal to or smaller than 1 μm . --

-- 5. (Amended) The semiconductor wafer according to Claim 2, wherein the dot [marks are] mark is formed [at least] on either one of the upper and lower inclined faces. --